

IN THE CLAIMS

What is claimed is:

- 1 **1.** A memory circuit, comprising:
 - 2 a plurality of sense amplifier circuits having a predetermined pitch
 - 3 in a first direction; and
 - 4 a plurality of programmable element controlled devices, each
 - 5 programmable element controlled device fitting within the pitch and
 - 6 isolating at least one associated bitline from a corresponding sense
 - 7 amplifier circuit when disabled.

- 1 **2.** The memory circuit of claim 1, wherein:
 - 2 the programmable element controlled devices comprise n-channel
 - 3 insulated gate field effect (IGFET) transistors laid-out within the pitch of
 - 4 the corresponding sense amplifier.

- 1 **3.** The memory circuit of claim 2, wherein:
 - 2 each of programmable element controlled devices includes
 - 3 a first n-channel IGFET having a source-drain path coupled
 - 4 between a first bitline of a bitline pair and the corresponding sense
 - 5 amplifier circuit, and
 - 6 a second n-channel IGFET having a source-drain path coupled
 - 7 between a second bitline of the bitline pair and the corresponding sense

8 amplifier circuit.

1 **4.** The memory circuit of claim 1, wherein:

2 each bitline is coupled to a plurality of memory cells selected from
3 the group consisting of one transistor dynamic random access memory
4 (DRAM) type cells, magnetoresistive RAM (MRAM) cells, thyristor RAM
5 (TRAM) cells, and ferromagnetic RAM (FRAM) cells.

1 **5.** The memory circuit of claim 1, wherein:

2 the bitlines comprise folded bitline pairs, each bitline of a bitline pair
3 being arranged parallel and adjacent to one another.

1 **6.** The memory circuit of claim 1, wherein:

2 the bitlines comprise open bitline pairs, with one bitline of each pair
3 extending over one array section and the other bitline of each pair
4 extending over a different array section.

1 **7.** The memory circuit of claim 1, wherein:

2 the bitlines comprise unpaired bitlines, each coupled to a sense
3 amplifier circuit that also receives a reference value to compare with a
4 data signal provided by each bitline.

1 **8.** The memory circuit of claim 1, wherein:

2 the bitlines are arranged into logical groups each including a
3 plurality of bitline pairs; and
4 the programmable element controlled devices associated with each
5 logical group are commonly disabled in response to the same control
6 signal.

1 **9.** A method of reducing a standby current contribution in conductive lines of a
2 memory device, comprising the steps of:
3 providing at least one transistor between each of a plurality of
4 conductive lines arranged in a first direction within a memory cell array
5 and a corresponding circuit coupled to the conductive line;
6 programming a fuse-type element to generate a control signal first value if
7 an associated conductive line is determined to have a defect; and
8 disabling each transistor when the associated control signal has the
9 first value to prevent defect induced current from flowing through the
10 transistor with respect to the corresponding conductive line.

1 **10.** The method of claim 9, wherein:
2 the step of programming the fuse-type element is performed in a
3 wafer test procedure.

1 **11.** The method of claim 9, wherein:
2 the step of providing at least one transistor includes providing at

3 least one transistor between a bitline and a corresponding sense amplifier
4 circuit.

1 **12.** The method of claim 11, wherein:

2 the step of providing at least one transistor includes providing at
3 least one transistor between a bitline and an equalization circuit within the
4 sense amplifier circuit.

1 **13.** The method of claim 9, further including:

2 the step of providing at least one transistor includes providing at
3 least one transistor between a wordline and a corresponding wordline
4 driver circuit.

5

1 **14.** A circuit for reducing defect induced standby current in a memory device,
2 comprising:

3 a plurality of first conductive lines parallel to one another, each first
4 conductive line coupled to a plurality of memory cells in a memory cell
5 array;

6 a plurality of first circuits arranged on at least one side of the
7 memory array, each first circuit being associated with at least one
8 associated first conductive line and having a same first pitch in a first
9 direction; and

10 a plurality of first isolation circuits, each first isolation circuit

11 permanently isolating a corresponding first circuit from the associated at
12 least one first conductive line when activated and fitting within the first
13 pitch.

1 **15.** The circuit of claim 14, wherein:
2 the plurality of first conductive lines comprise bitlines commonly
3 coupled to memory cells of the same column in the memory cell array; and
4 the plurality of first circuits comprise sense amplifier circuits for
5 driving an associated bitline according to a data value on such bitline.

1 **16.** The circuit of claim 15, further including:
2 a plurality of wordlines parallel to one another, each wordline
3 coupled to memory cells of the same row;
4 a plurality of wordline driver circuits arranged on at least a second
5 side of the memory array, each wordline driver circuit coupled to at least
6 one of the wordlines and having the same pitch in a second; and
7 a plurality of second isolation circuits, each second isolation circuit
8 permanently isolating a corresponding wordline driver circuit from the
9 associated wordline when activated.

1 **17.** The circuit of claim 14; wherein:
2 the plurality of first conductive lines comprise wordlines commonly
3 coupled to memory cells of the same row in the memory cell array; and

4 the plurality of first circuits comprises wordline driver circuits for
5 driving an associated wordline according to an applied address value.

1 **18.** The circuit of claim 14, further including:

2 at least one fuse circuit for providing an activation signal according
3 to the state of at least one fuse-type element; and

4 each isolation circuit comprises at least one transistor having a gate
5 coupled to the activation signal.

1 **19.** The circuit of claim 18, wherein:

2 the isolation circuit includes a plurality of transistors having gates
3 commonly coupled to the activation signal.

1 **20.** The circuit of claim 18, wherein:

2 the fuse-type element is selected from the group consisting of: a
3 fusible link alterable to have a conducting or a non-conducting state, an
4 anti-fuse structure alterable to have a conducting or a non-conducting
5 state, an electrically programmable memory cell programmable to have a
6 conducting or a non-conducting state.